“Evaluation of a Self-Diagnosis Algorithm for Regular Structures”

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Abstract

Given a set N of n interconnected processors, some of which may be faulty, the so-called *system-level diagnosis* is aimed at identifying the faulty processors by analyzing the outcomes of the available inter-processor tests. Cases of regular or quasi-regular interconnection schemes deserve special interest since regular interconnection structures are widely adopted in large parallel machines, and they appear suitable for application to wafer-scale IC-testing. This thesis introduces a general, efficient diagnosis algorithm (EDARS) for regular structures. This algorithm is derived by extending an algorithm for square grids developed by the same research group. The performance of EDARS, measured by the diagnosis correctness and the degree of diagnosis completeness, has been evaluated by means of extensive simulation. Simulation experiments, involving a wide range of regular structures, aim at evidencing to which extent performance of EDARS is influenced by some parameters characterizing the interconnection structure. Moreover, a worst-case condition for the correctness of diagnosis provided by EDARS when applied to hexagonal and octagonal grids is presented. Beside degree, whose influence could easily be expected, diameter and bisection width are also conjectured as possibly influencing the performance of EDARS. This conjecture is clearly supported by the simulation results reported in Chapters 5 and 6.